Vision for New India

"In the coming years, India will be biggest supplier of workforce to the world "

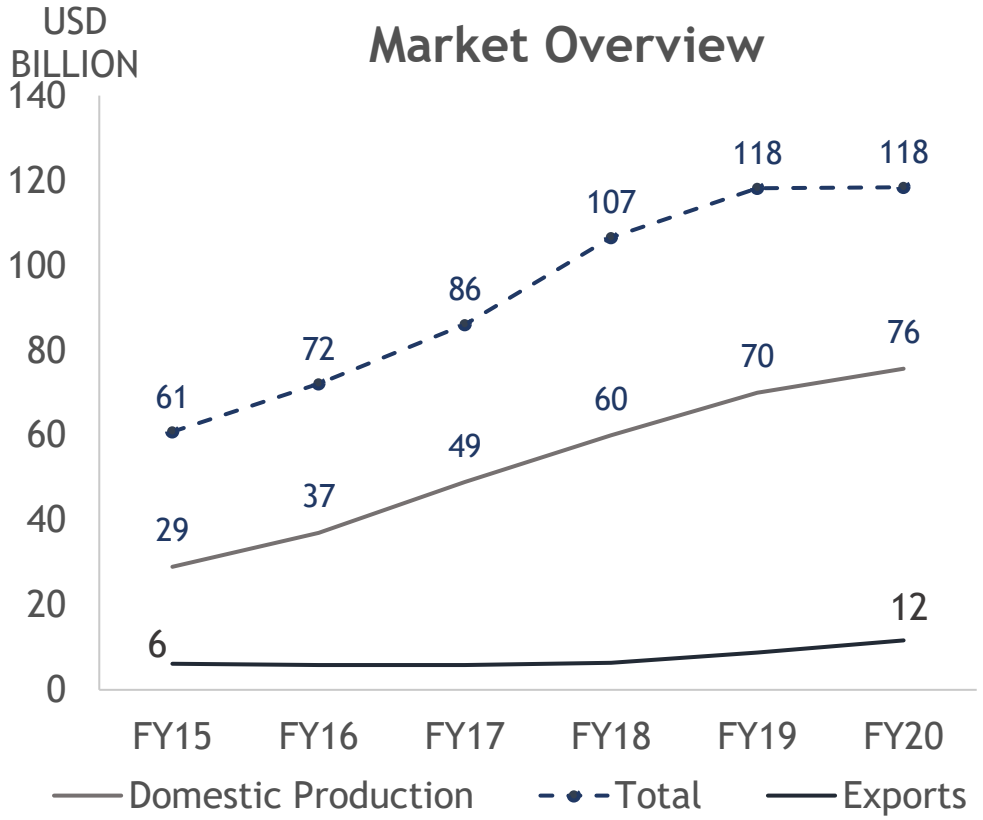
"The more we give importance to Skill development, the more competent will be our youth"

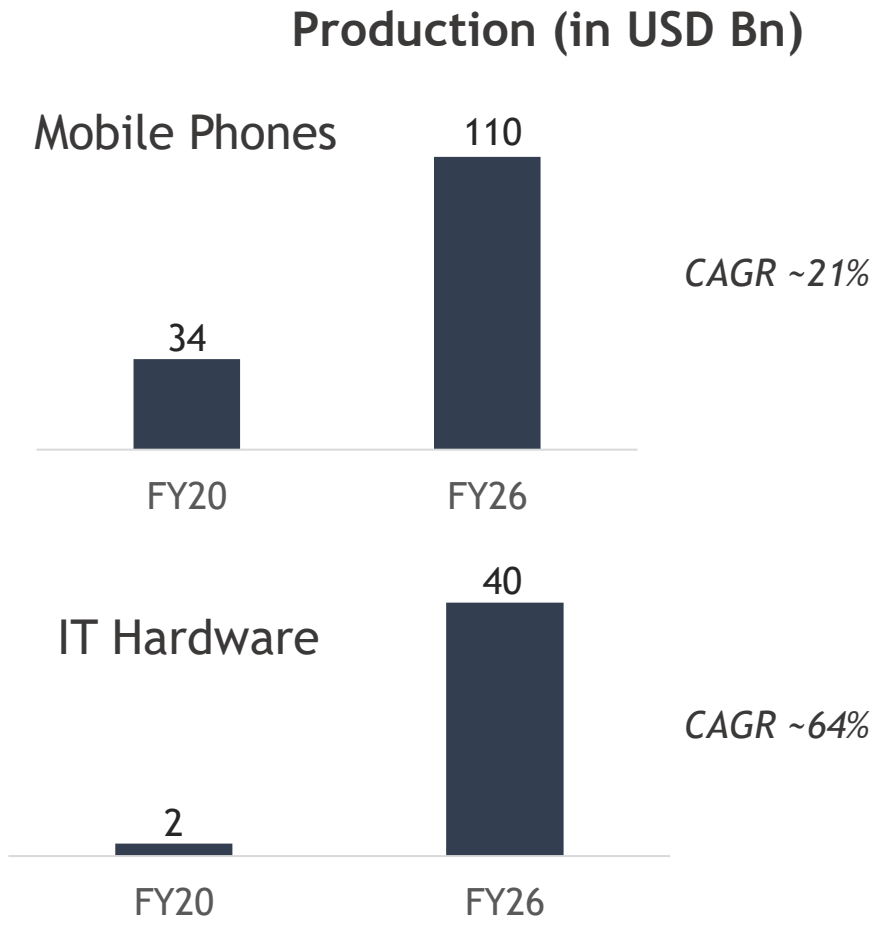
"Matching job creation with industry demand is the key to end unemployment "

" Design in India is as important as Make in India"

Shri Narendra Modi
Hon'ble Prime Minister of India

Electronics Manufacturing- USD 300 Bn Opportunity by 2025

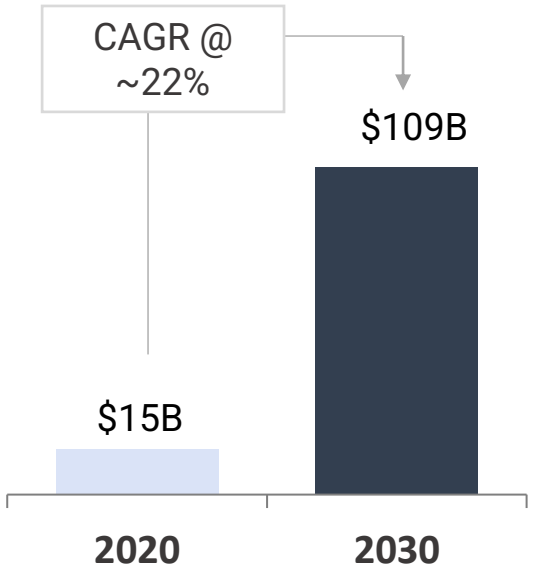




Source: Ministry of Electronics and Information Technology (MeitY)

Semicon India-
USD 110 Bn market opportunity by 2030

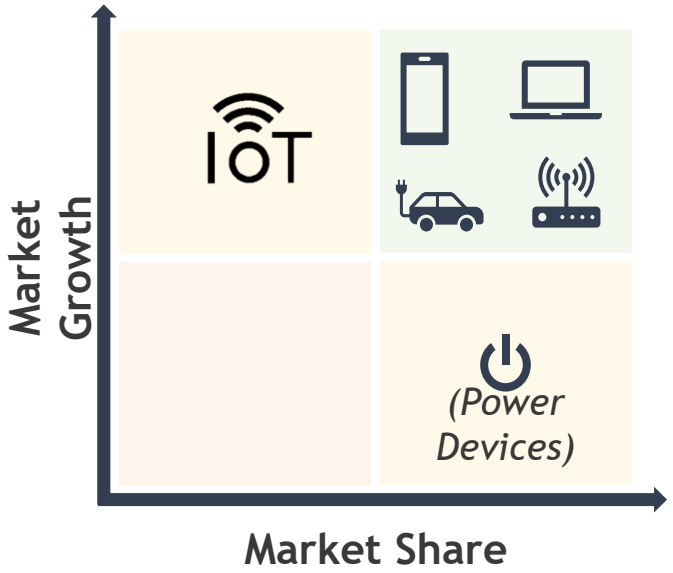
India Semiconductor Market



~10% of Global by 2030

Target Market:

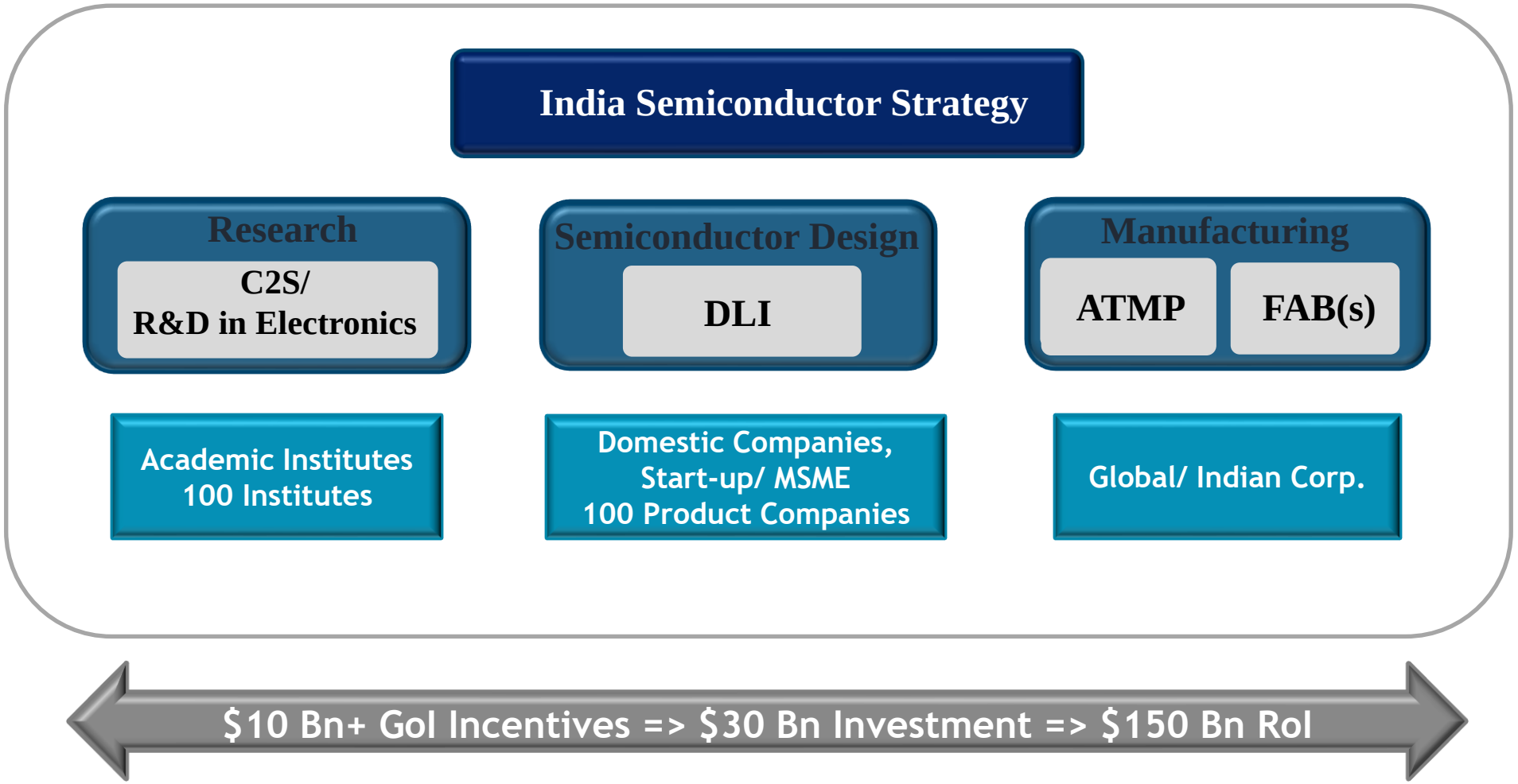
Auto + EV + Mobile + IT Hardware + Telecom



Auto, EV, Mobile, IT Hardware and Telecom high growth markets with large export potential

Source: IBS

India Semiconductor Strategy



Making India a Global Hub for Electronics Manufacturing : USD 30Bn in Fiscal Support

Support for Electronics Manufacturing

1. **Production Linked Incentives**	Mobile Phones, Components, IT Hardware
2. **Capex Linked Incentives**	Components, Sub-Assemblies
3. **Development of Electronics Manufacturing Clusters**	All Electronics Manufacturing

$7 Bn

Support for Semiconductor and Display Ecosystem

1. Semiconductor Fabs and Display Fabs
2. Compound Semiconductor and ATMP
3. Design Linked Incentive (DLI)
4. Modernization of Semi-conductor Laboratory (SCL)

$10 Bn

Support for Allied Sectors

Production Linked Incentives for

1. Advanced Chemistry Cell
2. Automobiles & Auto Components
3. Telecom & Networking
4. Solar PV Modules
5. White Goods

$13 Bn

Chips to Startup(C2S) Programme

"Fostering Next Generation Capabilities Among Chip Designers For Making India Self-Reliant In Electronics System Design"

Ministry of Electronics & Information Technology
Government of India

Digital India
Power To Empower

ELECTRONICS INDIA
Billion Needs Million Chips

Chips to Startup Programme

Background of Special Manpower Development (SMDP) Programme

1998-2005

SMDP-I

- **19 Institutions**
- **9300** Specialized Manpower in VLSI design

2005-2013

SMDP-II

- **32 Institutions**
- **28,000** Specialized Manpower in VLSI design
- **32 ASICs**

2014-2021

SMDP-C2SD

- **60 Institutions**
- **52,000** industry-ready manpower specialized in VLSI/ System design
- Working Prototype of **15 Systems/ 150 ASICs/ 30 FPGA based design**

2021-2026

C2S

- **100+ Institutions**
- **85,000** industry-ready manpower specialized in VLSI/ System design
- **20 Systems/175 ASICs/30 reusable IP Core/ 30 FPGA based design**
- Centralized National Infrastructure (Chip Centre)
- Incubation of **25** Start-up
- **10** ToTs

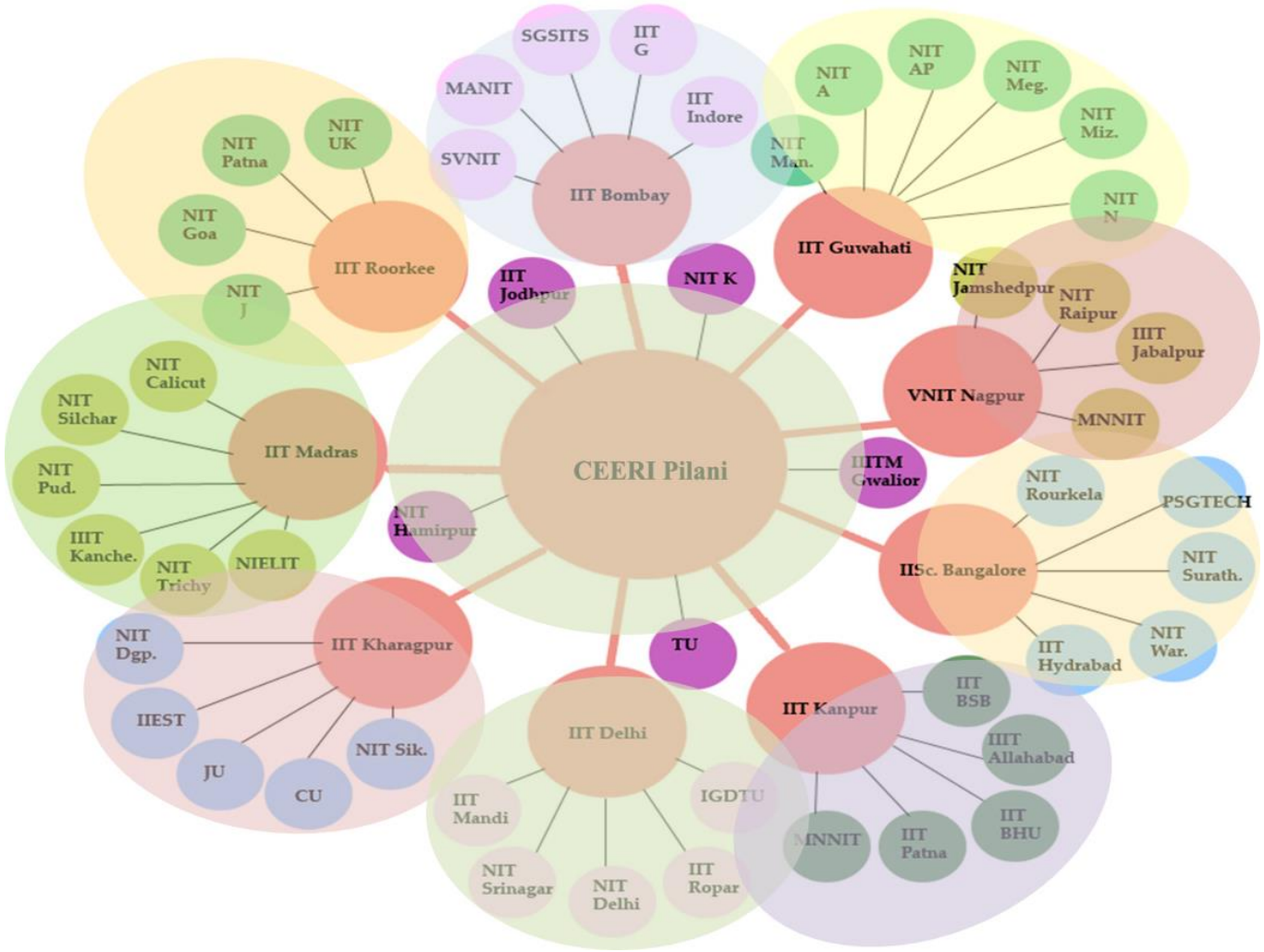
Advantage India

#1 20% of Global VLSI designers

#2 250+ Semiconductor Design companies

#3 2000+ Chips designed per year

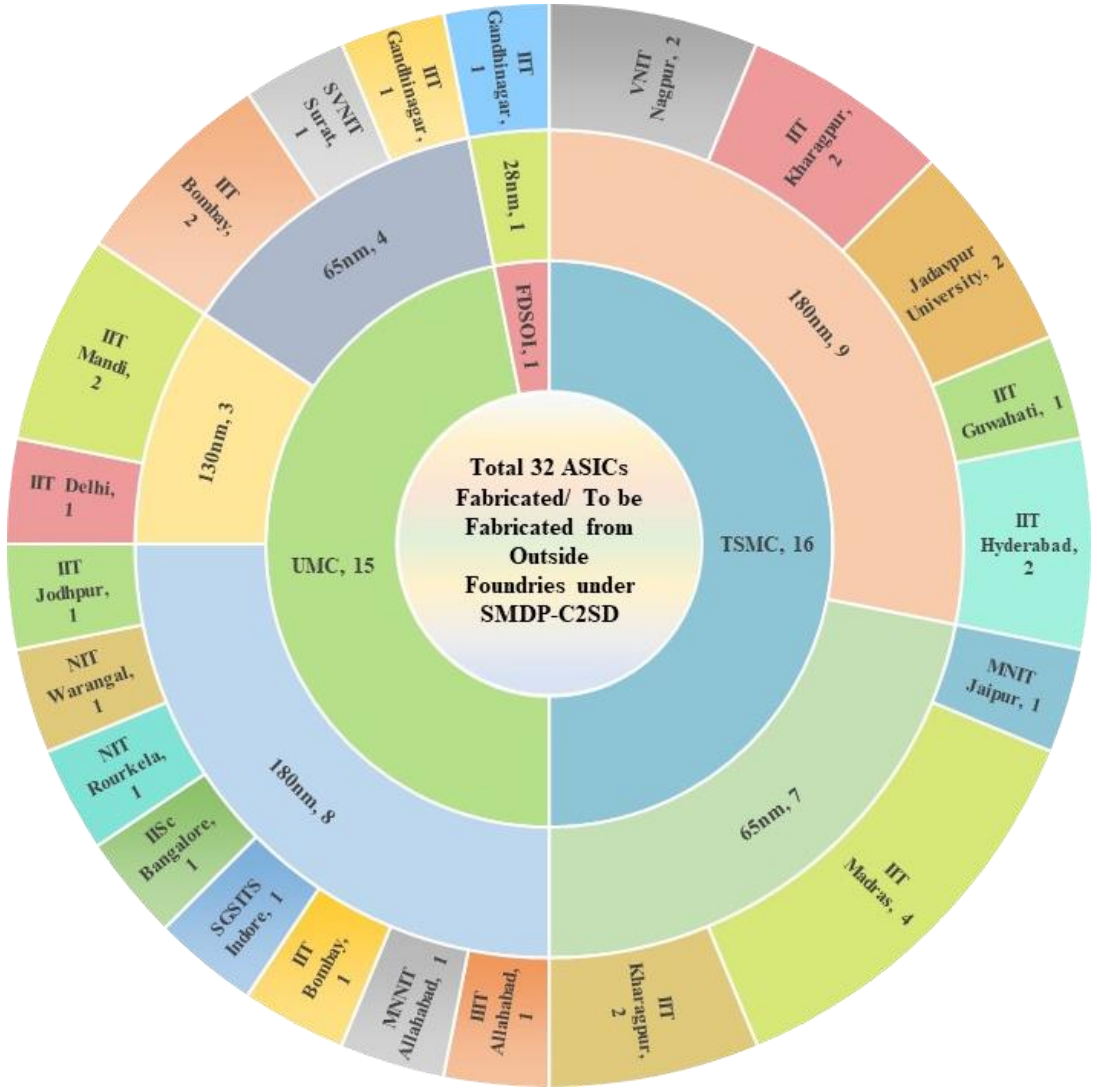
A Walkthrough of earlier SMDP-C2SD Programme



A Walkthrough of earlier SMDP-C2SD Programme

#	Cluster Project Title	RC	End User/ Application
1	ASIC for Next Generation LCA	IISc-B	DRDO & ISRO
2	Integrated microchip module for wireless capsule endoscopy	IIT-D	Healthcare
3	MAVI: Mobility Assistant for the Visually Impaired		Healthcare
4	Collision Detection in Automobiles using CMOS Imagers		Automotive
5	Wireless Sensor Node for Internet of Things (IoT)	VNIT-N	Railways
6	Low Power Speech Recognition System using a custom IC	IIT-M	Consumer Electronics
7	Array signal Processor ASIC		NPOL, DRDO
8	Wireless Sensor Node-System on Chip for monitoring of illegal activities	IIT-K	Forest Department of Odisha
9	RF Sensing of Cardiopulmonary Motion for survival detection under debris	IIT-R	NDRF Uttarakhand/ Disaster Management
10	System-on-Chip platform for Secured Speech Communication	CEERI	Strategic sector
11	FPGA/ASIC based Sensor Platform for Monitoring Air Pollutants	IIT-G	Assam Pollution Control Board
12	Versatile Data Acquisition & Signal Processing Platform for Seismic Application	IIT-Kgp	Disaster Management
13	Design and Implementation of variable data rate SerDes (up to 10 GBPS)		ISRO, DRDO
14	Versatile Physiological Signal Monitoring System	IIT-B	Healthcare
15	SerDes: High Speed Data Transceiver		SAC (ISRO)

A Walkthrough of earlier SMDP-C2SD Programme



Chips to Startup Programme

C2S Programme Objectives

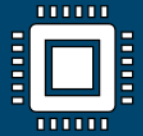
Chips to Startup Programme

Industry Ready Manpower Generation

For creating vibrant fabless chip design ecosystem in the country in System/ SoC Design area

Industry-Academia collaboration.

Promoting industry-led R&D, translational research



ASIC/ SoC/ Systems/IP Cores

Leapfrogging in ESDM space by way of **design & development**

Incubation of Startup

To inculcate the culture of entrepreneurship among students & researchers

C2S Programme Key Highlights

Chips to Startup Programme

C2S Support Mechanism

Chips to Startup Programme

1. Financial Support
2. Remote access to EDA Tools
3. FPGA Boards
4. Compute on Cloud
5. MPW Prototyping at FAB
6. Post-silicon validation support
7. Trainings on design flow
8. Internship opportunities
9. 200 PhD enrollment under Visvesvaraya PhD Scheme of MeitY

Eligible Applicants under C2S

Chips to Startup Programme

Academic Institutions

- IITs/IIITs/NITs/IISERs
- Institutions of National Importance/ Eminence
- Central/ Deemed Univ. under Central/State Govt.
- Private Univ./ Private Deemed Univ./Private Colleges

R&D Organizations

R&D Organizations/Institutions (with B.Tech /MTech/PhD courses)

MSMEs

M/o MSME notification dated 1st June 2020

Startups

DPIIT notification dated 19th Feb'2019

Key Application Areas (not limited to)

Chips to Startup Programme

Agriculture

Energy & Environment

HealthCare

Safety & Security

Strategic Sector

Intelligent Transport System

Emerging Technology

Disaster Management

Project Categorization

Chips to Startup Programme

CATEGORY – I

Design and Development of Systems/ SoCs/ ASICs/ Reusable IP Core

- Industry-Academia Collaborative Projects
- Duration: **Up to 3 Years**.
- Fund Support: **Up to Rs. 5 Crore per Proposal** (including fabrication cost) as per GFR norms.
- Fabrication Support: At any foundry in MPW Mode

Who Can Participate?

1. Academia/ R&D Organizations/ Domestic Startups/ MSME
2. Part funding from End User Organization (**preferably 10% (or more) of the overall budget (not kind)).**

Expected Outcomes

1. Targeted Technology Readiness Level **(TRL)-7 and above**.
2. System/ SoCs/ ASICs/ IP Cores

Project Categorization

Chips to Startup Programme

CATEGORY - II

Development of Application Oriented Working Prototype of IPs/ ASICs/ SoCs

- 40 Institutions in Consortium mode **(Consortium Size: maximum 5 Institutions)**
- Duration : **Up to 5 Years.**
- Fund Support: **Rs. 96 Lakh per Institution** as per GFR norms
- Fabrication Support: At any foundry in MPW Mode **(**depending on the needs of the project)

Who Can Participate?

1. Academia/ R&D organization (other than 10 Resource Centre of earlier SMDP-C2SD Programme)
2. **Letter of interest/ commitment** from End user organization.

Expected Outcomes

1. Targeted Technology Readiness Level **:TRL 7**
2. Working prototypes of silicon proven IPs / ASICs / SoCs/ Systems

Project Categorization

Chips to Startup Programme

CATEGORY - III

Proof of Concept oriented Research and Development of ASICs/FPGAs based Designs

- Individual ASIC/ FPGA/ COTS based development projects.
- 50 Government Institutions (mostly new).
- Duration : **5 Year**.
- Fund Support: **Rs. 86 Lakh per Institution** as per GFR norms
- Fabrication Support: **At SCL foundry** in MPW Mode

Who Can Participate?

1. SC/ST/Minority and Women University/ Institution (recognized by Government)
2. North East NITs/ IIITs
3. Government Institutions (including earlier SMDP-C2SD Category-III Institution).
4. Letter of interest from End user organizations.

Expected Outcomes

1. Targeted Technology Readiness Level : **TRL up to 4**.
2. Proof-of-Concept (PoC) of ASIC and FPGA based designs.

CDAC Bangalore Roles & Responsibilities

Chips to Startup Programme

- C-DAC Bangalore as Programme Coordination Institution for overall implementation of the programme
- Design Infrastructure support to participating Institutions including
  - Access to EDA tool grid
  - Access to Foundry for fabrication in MPW mode
  - Maintaining IP Core Repository
  - Fab compliance validation of designs, design flow and the Fab PDK
  - Chip Packaging support
  - Testing and Characterization support.
- As Design Centre, to streamline the adoption of a standardized VLSI design flow process among Academia and Start-ups.

Implementation Mechanism

Chips to Startup Programme

Submit

Proposal ❯ **Evaluation** ❯ **Approval** ❯ **GIA Release**

- Online Submission at www.c2s.gov.in (28th February, 2022)
- Acknowledgment mail issued

- Evaluation by Evaluation Committee

- Approval to Institutions for project initiation

- Millstones Linked GIA Releases through CDAC
- Facilitate Design Infrastructure support

C2S Web portal Important Links

Chips to Startup Programme

Guidelines

https://c2s.gov.in/guidelines.jsp

Eligibility Criteria

https://c2s.gov.in/eligibility.jsp

Proposal Format Download

https://c2s.gov.in/categorydownload.jsp

C2S Portal and Support Channels

Chips to Startup Programme

https://c2s.gov.in

support.c2s@cdac.in

support.c2s@meity.gov.in

Thank You