Vivado ML Enterprise Edition and Vitis Model Composer

What's New in 2023.2 Key Highlights

- Introducing Power Design Manager for Versal® ACAP & Kria™ SOM
- Intelligent Design Run now supported for Versal devices shows average 5% QoR improvement over explore strategy *
- 1.4X compile time speed-up for UltraScale+™ architecture designs with Incremental Compile Flow **
- Abstract Shell for DFX now supported for Versal devices and in project mode
- DFX support enabled for Versal Premium SSI devices

Vivado ML What's New by Category

Expand the sections below to learn more about the new features and enhancements in Vivado® ML 2022.2.

Device support

- Devices enabled in the Enterprise Edition of Vivado ML
    - Versal® Premium Series: XCVP1702, XCVP1802, XCVP1102
- Devices enabled in Standard and Enterprise Editions
    - Kria™ SOM: XCK24
- Devices that are production-ready
    - Versal Premium Series: XCVP1202
    - Versal Prime Series: XCVM1502
    - Versal AI Core Series: XCVC1702, XCVC1502

Install and licensing

- 25% reduction in peak disk footprint installation

IP enhancements

Infrastructure and Embedded

- Soft Endpoint Protection Unit (EPU) IP for protecting AXI agents residing in the PL

Storage

- Embedded RDMA enabled NIC (ERNIC) now supports up to 2k Queue Pairs (QP)

Gigabit Transceiver (GT) Wizard

- Versal GTMs now support rate switching between half and full density
- 16 configurations for Versal GTY/GTYP (limited to internal BRAM capacity)

Wired

- 100G Multi-rate Ethernet MAC Subsystems (MRMAC)
    - Enabled 100G Ethernet 106G serial lane support
- 600G Multi-rate Ethernet MAC Subsystem (DCMAC)
    - Enabled 100GE, 200GE, 400GE 106G serial per lane support
- Aurora 64B/66B
    - Added support for 16 lanes of GTYP or Gigabit Transceiver Module (GTM) on Versal Premium

Wireless

- Zynq® RFSoC DFE IP Update: Channel Filter and DUC-DDC UL/DL sharing

- Zynq® RFSoC DFE DPD Update: PL resource reduction
- Zynq® RFSoC DFE O-RU TRD: Updated w/ Low PHY processing only

PCIe® Subsystems

- CPM5 x86 host drivers for Linux and DPDK in public release on GitHub
- Versal CPM5 PCIe BMD Simulation Design (from CED Store)
- Versal CPM Tandem PCIe Design (from CED Store)
- QDMA v5.0 improved performance/resource utilization

Multimedia

- Versal AI Edge enablement of soft IPs and Video Decoder Unit (VDU)
- Warp Processor IP in production
- Ultra HD 8K multimedia solution enablement for
    - HDMI2.1
    - Video Mixer IP

IP Integrator

- AXI streaming NoC MxN support in IP Integrator
- New address remap feature
- Vivado for default syntax checking
- Address path visualization
- XML to JSON format for XCI files

Simulation

- Support for System Verilog “Interface Class”
- Debug support for reference type System Verilog objects via tcl command and object window
- VHDL-2008 support

Hardware debug

- Support for PCIe Debugger on new Versal architectures
    - VP1502
    - VP1702
    - VP1802
- HBM2E Debugger support on Versal HBM devices
- Integrated Bit Error Ratio Tester (IBERT) support on new Versal architectures
    - VP1502
    - VP1702
    - VP1802

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Implementation

- QoR optimization for high fanout nets
- Placer replication for hard IP blocks
- Two new partitioning constraints for SSI designs
- LUT decomposition option to reduce congestion
- Incremental implementation enabled for monolithic Versal devices
- Support ECO flow for Versal devices

Timing closure

- New content added to QoR assessment report
- Average 5% QoR improvement for Versal designs when Intelligent Design Runs is enabled

DFX

- DFX support for SSI devices
- Abstract Shell support for Versal Premium and Versal HBM devices
- Abstract Shell support for project-based mode

Vitis Model Composer Overview

Vitis™ Model Composer is a model-based design tool that enables rapid design exploration within the MathWorks MATLAB® and Simulink® environment and accelerates the path to production on AMD devices through automatic code generation.

You can design your DSP algorithms and iterate through them using high-level, performance-optimized blocks and validate functional correctness through system-level simulations. Vitis Model Composer transforms your design into a production-quality implementation through automatic optimizations.

The tool provides a library of more than 200 HDL, HLS, and AI Engine blocks for the design and implementation of algorithms on AMD devices. It also enables importing custom HDL, HLS, and AI Engine code as blocks into the tool.

Vitis Model Composer offers a way to design the Versal™ adaptive SoCs. The tool can help designers create complex systems targeting both the PL and the AI Engine array. Learn how to use Versal AI Engines with Vitis Model Composer.

Vitis Model Composer includes all the functionality of AMD System Generator for DSP, which is no longer shipped as a standalone tool since 2021.1.

Analysis, Debugging & Visualization

Use the MATLAB and Simulink environment to analyze and visualize your design:

- Use optimized AI Engine, HLS, and HDL blocks directly from the Simulink library browser
- Import custom AI Engines, HLS, and HDL code as blocks
- Run fast simulations in the Simulink environment
- Compare the results with golden references in the MATLAB and Simulink environment
- Tap into intermediate signals to debug and get visibility into the design

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Co-Simulation of AI Engines and Adaptable Engines

Co-simulate a heterogeneous system:

- Directly use optimized AI Engines/HLS/Adaptable Engines from the library browser or import code as blocks
- Seamlessly connect AI Engine arrays with HLS kernel blocks or HDL blocks

Code Generation

Increase productivity by generating code from your design:

- Generate graph code along with constraints
- Generate RTL (Verilog/VHDL)
- Generate optimized HLS code with inserted pragmas
- Generate a test bench

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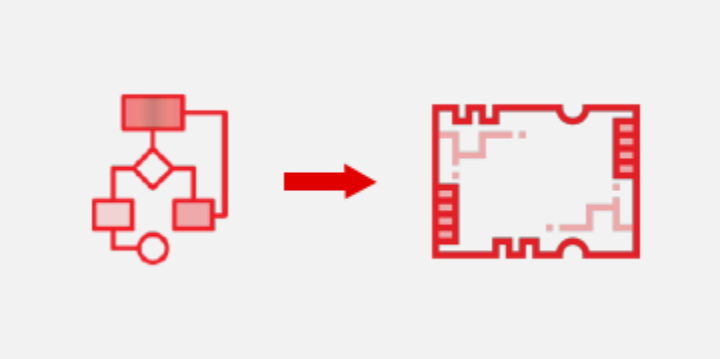
Validation of Design in Hardware



Easily validate your design in hardware:

- Generate data movers, processing system code, config files
- Generate the make files to build the design for hardware
- Move the design into hardware with a click of a button

AI Engine block updates

- Support for importing AIE-ML graphs as blocks into Vitis Model Composer
- New DSPlib functions for AIE and AIE-ML implementation in Vitis Model Composer
- Plotting of AIE simulator output for internal signals in the Simulink® tool

HLS Kernel block updates

- Automatic test bench generation
- Expanded data type support for HLS Kernel blocks

Integration of Vitis Model Composer and Vitis tool

- Generation of .xo and libadf.a files directly from Vitis Model Composer

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